IN THE CLAIMS

1-18. (Canceled)

19. (Currently Amended) A method comprising:

storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations; and

duplicating bits from the plurality of non-contiguous groups of destination [[bits ]]storage locations into groups of destination storage locations ~~contiguous~~ adjacent to the non-contiguous groups of destination storage locations.

20. (Previously Presented) The method of claim 19 in which the source bits are stored in a first register.

21. (Previously Presented) The method of claim 19 in which the source bits represent a double-precision floating point value.

22. (Previously Presented) The method of claim 19 in which the source bits are stored in a first memory location.

23. (Previously Presented) The method of claim 19 in which the source bits represent a single-precision floating point value.

24-92. (Canceled)

93. (Currently Amended) An apparatus comprising:

a first storage area to store a plurality of non-contiguous groups of source bits in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into a plurality of non-contiguous groups of destination storage locations; and

a second storage area to store contiguous duplicates of the plurality of non-contiguous groups of source bits into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.

94. (Previously Presented) The apparatus of claim 93, wherein the plurality of non-contiguous groups of source bits are to represent a plurality of 32-bit double-precision floating point value.

95. (Previously Presented) The apparatus of claim 94, wherein the first storage area comprises a 128-bit memory location.

96. (Previously Presented) The apparatus of claim 94, wherein the first storage and second storage areas each comprise a 128-bit register.

97. (Previously Presented) The apparatus of claim 93, wherein the plurality of non-contiguous groups of source bits comprises comprise four single-precision floating point values.

98. (Previously Presented) The apparatus of claim 93, wherein the second storage area is to store only two of the plurality of non-contiguous groups of source bits and their duplicates.

99. (Previously Presented) The apparatus of claim 93, wherein the first and second storage areas are to store data corresponding to multi-media instructions.

100. (Previously Presented) The apparatus of claim 99, further comprising an execution unit to execute the multi-media instructions.

101. (Currently Amended) A system comprising:

a memory to store a plurality of instructions;

a processor to fetch a first instruction from the memory, wherein the first instruction, if executed by the processor, is to cause the processor to store contiguous duplicates of a plurality of non-contiguous groups of source bits into a plurality of groups of destination storage locations without the first instruction specifying an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of groups of destination storage locations.

102. (Previously Presented) The system of claim 101, wherein the plurality of non-contiguous groups of source bits include a least significant 32 source bits.

103. (Previously Presented) The system of claim 101, wherein the plurality of non-contiguous groups of source bits include a most significant 32 source bits.

104. (Previously Presented) The system of claim 102, wherein the plurality of non-contiguous groups of source bits include a second most significant group of 32 source bits.

105. (Previously Presented) The system of claim 103, wherein the plurality of non-contiguous groups of source bits include a second least-significant group of 32 source bits.

106. (Canceled)

107. (Previously Presented) The system of claim 105, wherein the first instruction is a MOVSHDUP instruction.

108. (Previously Presented) The system of claim 104, wherein the first instruction is a MOVSLDUP instruction.

109. (Previously Presented) The system of claim 101, wherein the processor is to fetch a second instruction from the memory, the second instruction to store a first number of non-contiguous duplicates of a second number of contiguous groups of source bits into a destination storage location, the first number being larger than the second number.

110. (Previously Presented) A machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;

storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register.

111. (Previously Presented) The machine-readable medium of claim 110 wherein the source value is stored in a memory location.

112. (Previously Presented) The machine-readable medium of claim 110, wherein the source value is stored in a register.

113. (Previously Presented) A machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [31-0] and [63-32] of a destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register.

114. (Previously Presented) The machine-readable medium of claim 113 wherein the source value is stored in a memory location.

115. (Previously Presented) The machine-readable medium of claim 113, wherein the source value is stored in a register.

116. (Previously Presented) A machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:

storing only bits [63-32] of a source value into bit storage locations [127-96] and [63-32] of a destination register;

storing only bits [31-0] of the source value into bit storage locations [31-0] and [95-64] of the destination register, wherein the instruction does not include a code

to designate the order in which the source bits are to be stored in the destination register.

117. (Previously Presented) The machine-readable medium of claim 116 wherein the source value is stored in a memory location.

118. (Previously Presented) The machine-readable medium of claim 116, wherein the source value is stored in a register.